Quad Supply Voltage Supervisor with Adjustable Delay and Watchdog Timer

Check for Samples: TPS386000, TPS386020, TPS386040, TPS386060

FEATURES

- **Four Independent Voltage Supervisors**
- **Channels 1, 2, 3: Adjustable Threshold Down to 0.4V**
- **Channel 4: Adjustable Threshold at Any Positive/Negative Voltage**
- **Adjustable Delay Time: 1.4ms to 10s**
- **Threshold Accuracy: 0.25% typ**
- **Very Low Quiescent Current: 11µA typ**
- **Channel 1: Manual Reset ($\overline{MR}$) Input**
- **Channel 4: Window Comparator**
- **Watchdog Timer with Dedicated Output**
- **Well-Controlled Output During Power-Up**
- **TPS386000: Open-Drain $\overline{RESETn}$ and $\overline{WDO}$**
- **TPS386020: Open-Drain RESETn and WDO**
- **TPS386040: Push-Pull $\overline{RESETn}$ and $\overline{WDO}$**
- **TPS386060: Push-Pull RESETn and WDO**
- **Package: 4mm x 4mm, 20-pin QFN**

APPLICATIONS

- **All DSP and Microcontroller Applications**
- **All FPGA/ASIC Applications**
- **Telecom/Wireless Infrastructure**
- **Industrial Equipment**
- **Analog Sequencing**

DESCRIPTION

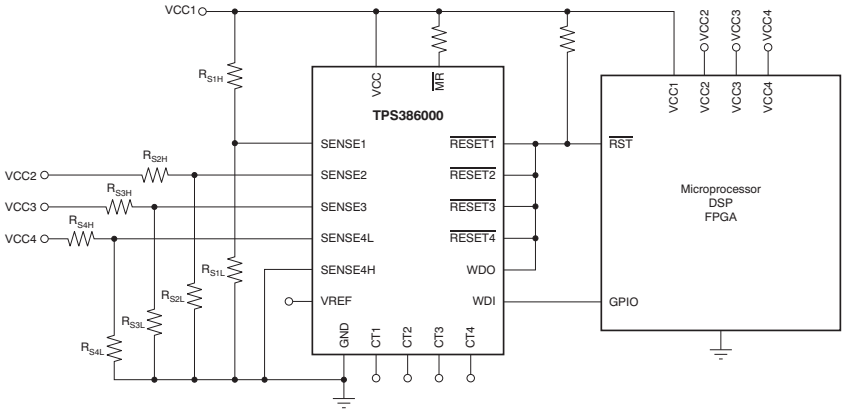
The TPS3860x0 family of supply voltage supervisors (SVSs) can monitor four power rails that are greater than 0.4V and one power rail less than 0.4V (including negative voltage) with a 0.25% (typical) threshold accuracy. Each of the four supervisory circuits (SVS-n) assert a $\overline{RESETn}$ or RESETn output signal when the SENSEm input voltage drops below the programmed threshold. With external resistors, the threshold of each SVS-n can be programmed (where *n* = 1, 2, 3, 4 and *m* = 1, 2, 3, 4L, 4H).

Each SVS-n has a programmable delay before releasing $\overline{RESETn}$ or RESETn. The delay time can be set independently for each SVS from 1.4ms to 10s through the CTn pin connection. Only SVS-1 has an active-low manual reset ($\overline{MR}$) input; a logic-low input to $\overline{MR}$ asserts $\overline{RESET1}$ or RESET1.

SVS-4 monitors the threshold window using two comparators. The extra comparator can be configured as a fifth SVS to monitor negative voltage with voltage reference output VREF.

The TPS3860x0 has a very low quiescent current of 11µA (typical) and is available in a small, 4mm x 4mm, QFN-20 package.

TPS386000 Typical Application Circuit



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	DESCRIPTION
TPS3860**x**0**yyy***z*	**x** is device configuration option **x** = 0: Open-drain, active low **x** = 2: Open-drain, active high **x** = 4: Push-pull, active low **x** = 6: Push-pull, active high **yyy** is package designator **z** is package quantity

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating junction temperature range, unless otherwise noted.

		TPS3860x0	UNIT
Input voltage range, V_{VCC}		–0.3 to 7.0	V
CT pin voltage range, V_{CT1}, V_{CT2}, V_{CT3}, V_{CT4}		–0.3 to V_{VCC} + 0.3	V
Other voltage ranges: V_{RESET1}, V_{RESET2}, V_{RESET3}, V_{RESET4}, V_{MR}, V_{SENSE1}, V_{SENSE2}, V_{SENSE3}, $V_{SENSE4L}$, $V_{SENSE4H}$, V_{WDI}, V_{WDO}		–0.3 to 7.0	V
$\overline{\text{RESETn}}$, RESETn, $\overline{\text{WDO}}$, WDO, VREF pin current		5	mA
Continuous total power dissipation		See *Dissipation Ratings Table*	
Operating virtual junction temperature range, T_J (2)		–40 to +150	°C
Operating ambient temperature range		–40 to +125	°C
Storage temperature range, T_{STG}		–65 to +150	°C
ESD rating	Human body model (HBM)	2	kV
	Charged device model (CDM)	500	V

(1) Stresses beyond those listed under the *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under the recommended operating conditions is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
(2) As a result of the low dissipated power in this device, it is assumed that $T_J = T_A$.

DISSIPATION RATINGS

PACKAGE	T_A < +25°C POWER RATING	DERATING FACTOR ABOVE T_A > +25°C	T_A = +70°C POWER RATING	T_A = +85°C POWER RATING
RGP	2.86W	28.6mW/°C	1.57W	1.24W

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ELECTRICAL CHARACTERISTICS

Over the operating temperature range of T_J = –40°C to +125°C, 1.8V < V_{VCC} < 6.5V, R_{RESETn} (*n* = 1, 2, 3, 4) = 100kΩ to V_{VCC} (TPS386000, TPS386020 only), C_{RESETn} (*n* = 1, 2, 3, 4L, 4H) = 50pF to GND, R_{WDO} = 100kΩ to V_{VCC}, C_{WDO} = 50pF to GND, V_{MR} = 100kΩ to V_{VCC}, WDI = GND, and CTn (*n* = 1, 2, 3, 4) = open, unless otherwise noted. Typical values are at T_J = +25°C.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{VCC}	Input supply range			1.8		6.5	V
I_{VCC}	Supply current (current into VCC pin)		V_{VCC} = 3.3V, $\overline{\text{RESETn}}$ or RESETn not asserted, WDI toggling(1), no output load, and VREF open		11	19	µA
			V_{VCC} = 6.5V, $\overline{\text{RESETn}}$ or RESETn not asserted, WDI toggling(1), no output load, and VREF open		13	22	µA
	Power-up reset voltage(2)(3)	TPS386000, TPS386040	V_{OL} (max) = 0.2V, I_{RESETn} = 15µA			0.9	V
V_{ITN}	Negative-going input threshold voltage		SENSE1, SENSE2, SENSE3, SENSE4L	396	400	404	mV
V_{ITP}	Positive-going input threshold voltage		SENSE4H	396	400	404	mV
V_{HYSN}	Hysteresis (positive-going) on V_{ITN}		SENSE1, SENSE2, SENSE3, SENSE4L		3.5	10	mV
V_{HYSP}	Hysteresis (negative-going) on V_{ITP}		SENSE4H		3.5	10	mV
I_{SENSE}	Input current at SENSEm pin		V_{SENSEm} = 0.42V	–25	±1	+25	nA
I_{CT}	CTn pin charging current	CT1	C_{CT1} > 220pF, V_{CT1} = 0.5V(4)	245	300	355	nA
		CT2, CT3, CT4	C_{CTn} > 220pF, V_{CTn} = 0.5V(4)	235	300	365	nA
$V_{TH(CTn)}$	CTn pin threshold		C_{CTn} > 220pF	1.180	1.238	1.299	V
V_{IL}	$\overline{\text{MR}}$ and WDI logic low input			0		0.3V_{VCC}	V
V_{IH}	$\overline{\text{MR}}$ and WDI logic high input			0.7V_{VCC}			V
V_{OL}	Low-level $\overline{\text{RESETn}}$ or RESETn output voltage	All	I_{OL} = 1mA			0.4	V
		TPS386000, TPS386040	SENSEn = 0V, 1.3V < V_{VCC} < 1.8V, I_{OL} = 0.4mA(2)			0.3	V
	Low-level WDO output voltage	All	I_{OL} = 1mA			0.4	V
		TPS386020, TPS386060	SENSEn = 0V, 1.3V < V_{VCC} < 1.8V, I_{OL} = 0.4mA(2)			0.3	V
V_{OH}	High-level $\overline{\text{RESETn}}$ or RESETn output voltage	TPS386040, TPS386060	I_{OL} = –1mA	V_{VCC} – 0.4			V
		TPS386060	SENSEn = 0V, 1.3V < V_{VCC} < 1.8V, I_{OL} = –0.4mA(2)	V_{VCC} – 0.3			V
	High-level WDO output voltage	TPS386040, TPS386060	I_{OL} = –1mA	V_{VCC} – 0.4			V
		TPS386040	SENSEn = 0V, 1.3V < V_{VCC} < 1.8V, I_{OL} = –0.4mA(2)	V_{VCC} – 0.3			V
I_{LKG}	$\overline{\text{RESETn}}$, RESETn, $\overline{\text{WDO}}$, and WDO leakage current	TPS386000, TPS386020	V_{RESETn} = 6.5V, $\overline{\text{RESETn}}$, RESETn, $\overline{\text{WDO}}$, and WDO are logic high	–300		300	nA
V_{REF}	Reference voltage output		1µA < I_{VREF} < 0.2mA (source only, no sink)	1.18	1.20	1.22	V
C_{IN}	Input pin capacitance		CTn: 0V to V_{VCC}, other pins: 0V to 6.5V		5		pF
t_W	Input pulse width to SENSEm and $\overline{\text{MR}}$ pins		SENSEm: 1.05V_{ITN} → 0.95V_{ITN} or 0.95V_{ITP} → 1.05V_{ITP}		4		µs
			$\overline{\text{MR}}$: 0.7V_{CC} → 0.3V_{VCC}		1		ns
t_D	$\overline{\text{RESETn}}$ or RESETn delay time		CTn = open	14	20	24	ms
			CTn = V_{VCC}	225	300	375	ms
t_{WDT}	Watchdog timer timeout period		Start from $\overline{\text{RESET1}}$ or RESET1 release or last WDI transition	450	600	750	ms

(1) Toggling WDI for a period less than t_{WDT} negatively affects I_{VCC}.
(2) These specifications are beyond the recommended V_{VCC} range, and only define $\overline{\text{RESETn}}$ or RESETn output performance during VCC ramp up.
(3) The lowest supply voltage (V_{VCC}) at which $\overline{\text{RESETn}}$ or RESETn becomes active; t_{RISE}(VCC) ≥ 15µs/V.
(4) CTn (where *n* = 1, 2, 3, or 4) are constant current charging sources working from a range of 0V to $V_{TH(CTn)}$, and the device is tested at V_{CTn} = 0.5V. For I_{CT} performance between 0V and $V_{TH(CTn)}$, see Figure 25.

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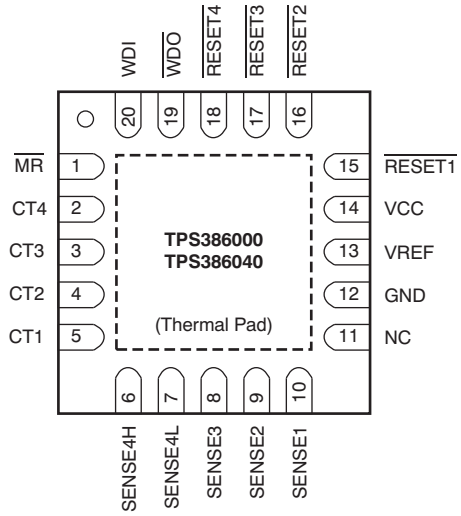
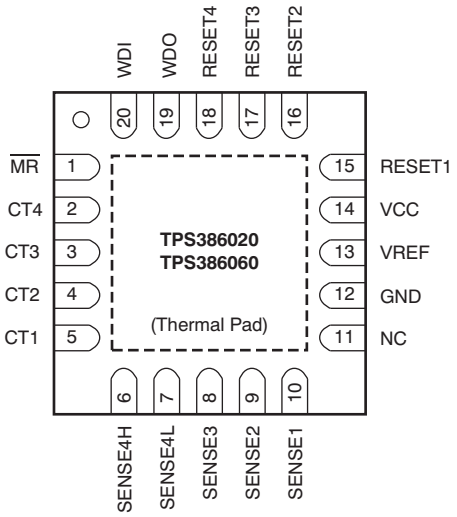
PIN CONFIGURATIONS

RGP PACKAGE
QFN-20
(TOP VIEW)





PIN ASSIGNMENTS

PIN		DESCRIPTION	
NAME	NO.		
VCC	14	Supply voltage. Connecting a 0.1µF ceramic capacitor close to this pin is recommended.	
GND	12	Ground	
SENSE1	10	Monitor voltage input to SVS-1	When the voltage at this terminal drops below the threshold voltage (V_{ITN}), $\overline{\text{RESET1}}$ is asserted.
SENSE2	9	Monitor voltage input to SVS-2	When the voltage at this terminal drops below the threshold voltage (V_{ITN}), $\overline{\text{RESET2}}$ is asserted.
SENSE3	8	Monitor voltage input to SVS-3	When the voltage at this terminal drops below the threshold voltage (V_{ITN}), $\overline{\text{RESET3}}$ is asserted.
SENSE4L	7	Falling monitor voltage input to SVS-4. When the voltage at this terminal drops below the threshold voltage (V_{ITN}), $\overline{\text{RESET4}}$ or RESET4 is asserted.	
SENSE4H	6	Rising monitor voltage input to SVS-4. When the voltage at this terminal exceeds the threshold voltage (V_{ITP}), $\overline{\text{RESET4}}$ or RESET4 is asserted. This pin can also be used to monitor the negative voltage rail in combination with VREF pin. Connect to GND if not being used.	
CT1	5	Reset delay programming pin for SVS-1	Connecting this pin to VCC through a 40kΩ to 200kΩ resistor, or leaving it open, selects a fixed delay time (see the Electrical Characteristics). Connecting a capacitor > 220pF between this pin and GND selects the programmable delay time (see the Reset Delay Time section).
CT2	4	Reset delay programming pin for SVS-2	
CT3	3	Reset delay programming pin for SVS-3	
CT4	2	Reset delay programming pin for SVS-4	
VREF	13	Reference voltage output. By connecting a resistor network between this pin and the negative power rail, SENSE4H can monitor the negative power rail. This pin is intended to only source current into resistor(s). Do not connect resistor(s) to a voltage higher than 1.2V. Do not connect only a capacitor.	
$\overline{\text{MR}}$	1	Manual reset input for SVS-1. Logic low level of this pin asserts $\overline{\text{RESET1}}$ or RESET1.	
WDI	20	Watchdog timer (WDT) trigger input. Inputting either a positive or negative logic edge every 610ms (typ) prevents WDT time out at the $\overline{\text{WDO}}$ or WDO pin. Timer starts from releasing event of $\overline{\text{RESET1}}$ or RESET1.	
NC	11	Not connected. It is recommended to connect this pin to the GND pin (pin 12), which is next to this pin.	
(Thermal Pad)	(PAD)	This is the IC substrate. This pad must be connected only to GND or to the floating thermal pattern on the printed circuit board (PCB).	

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PIN ASSIGNMENTS (continued)

PIN		DESCRIPTION	
NAME	NO.		
TPS386000			
$\overline{\text{RESET1}}$	15	Active low reset output of SVS-1	$\overline{\text{RESETn}}$ is an open-drain output pin. When $\overline{\text{RESETn}}$ is asserted, this pin remains in a low-impedance state. When $\overline{\text{RESETn}}$ is released, this pin goes to a high-impedance state after the delay time programmed by CTn.
$\overline{\text{RESET2}}$	16	Active low reset output of SVS-2	
$\overline{\text{RESET3}}$	17	Active low reset output of SVS-3	
$\overline{\text{RESET4}}$	18	Active low reset output of SVS-4	
$\overline{\text{WDO}}$	19	Watchdog timer output. This is an open-drain output pin. When WDT times out, this pin goes to a low-impedance state to GND. If there is no WDT timeout, this pin stays in a high-impedance state.	
TPS386020			
RESET1	15	Active high reset output of SVS-1	RESETn is open-drain output pin. When RESETn is asserted, this pin remains in a high impedance state. When RESETn is released, this pin goes to a low-impedance state after the delay time programmed by CTn.
RESET2	16	Active high reset output of SVS-2	
RESET3	17	Active high reset output of SVS-3	
RESET4	18	Active high reset output of SVS-4	
WDO	19	Watchdog timer output. This is an open-drain output pin. When WDT times out, this pin goes to a high-impedance state. If there is no WDT timeout, this pin stays in a low-impedance state to GND.	
TPS386040			
$\overline{\text{RESET1}}$	15	Active low reset output of SVS-1	$\overline{\text{RESETn}}$ is a push-pull logic buffer output pin. When $\overline{\text{RESETn}}$ is asserted, this pin remains logic low. When $\overline{\text{RESETn}}$ is released, this pin goes to logic high after the delay time programmed by CTn.
$\overline{\text{RESET2}}$	16	Active low reset output of SVS-2	
$\overline{\text{RESET3}}$	17	Active low reset output of SVS-3	
$\overline{\text{RESET4}}$	18	Active low reset output of SVS-4	
$\overline{\text{WDO}}$	19	Watchdog timer output. This is a push-pull output pin. When WDT times out, this pin goes to logic low. If there is no WDT timeout, this pin stays in logic high.	
TPS386060			
RESET1	15	Active high reset output of SVS-1	RESETn is a push-pull logic buffer output pin. When RESETn is asserted, this pin remains logic high. When RESETn is released, this pin goes to logic low after the delay time programmed by CTn.
RESET2	16	Active high reset output of SVS-2	
RESET3	17	Active high reset output of SVS-3	
RESET4	18	Active high reset output of SVS-4	
WDO	19	Watchdog timer output. This is a push-pull output pin. When WDT times out, this pin goes to logic high. If there is no WDT timeout, this pin stays in logic low.	

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FUNCTIONAL BLOCK DIAGRAMS

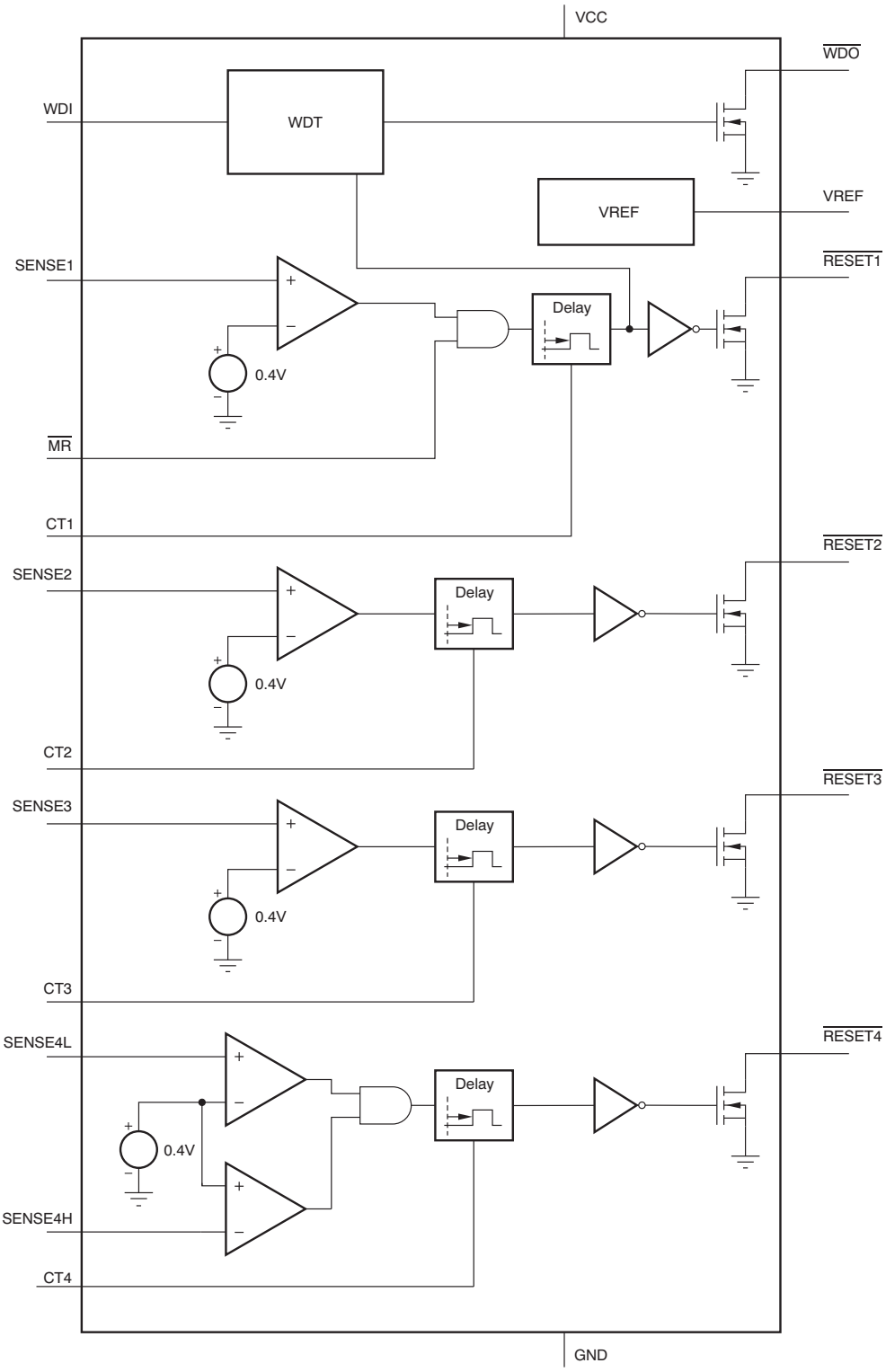

Figure 1. TPS386000 Block Diagram

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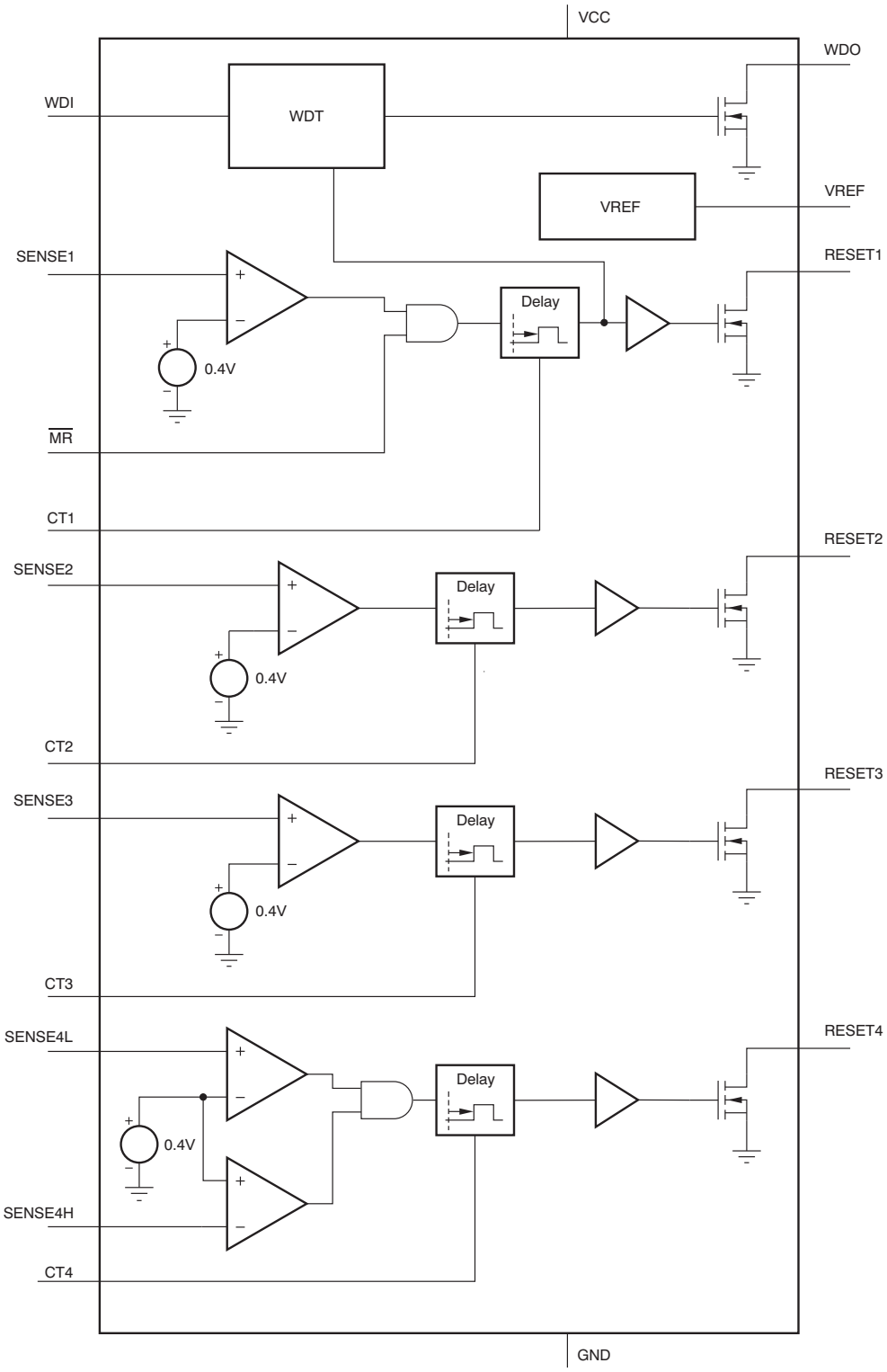

Figure 2. TPS386020 Block Diagram

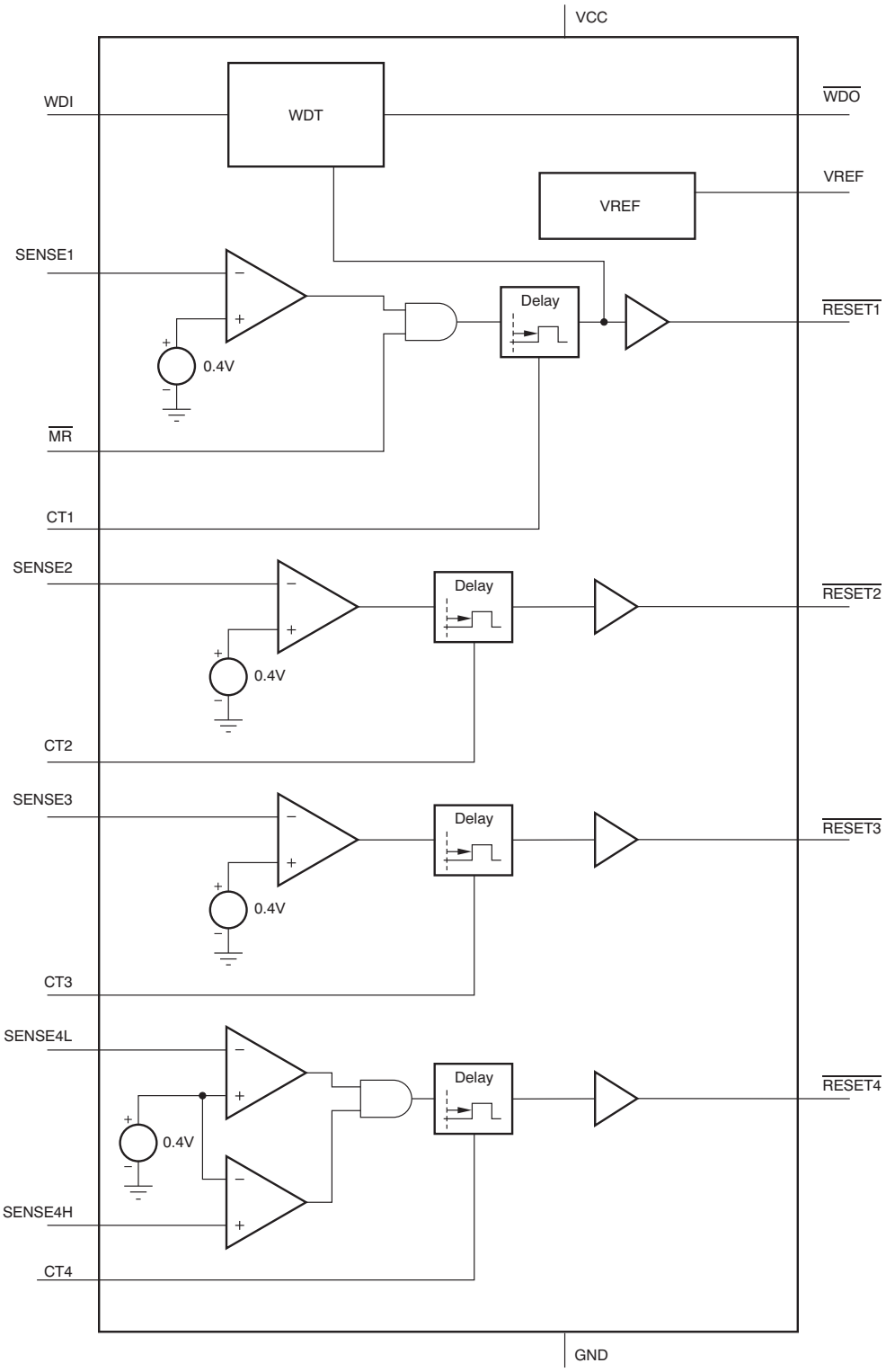

Figure 3. TPS386040 Block Diagram

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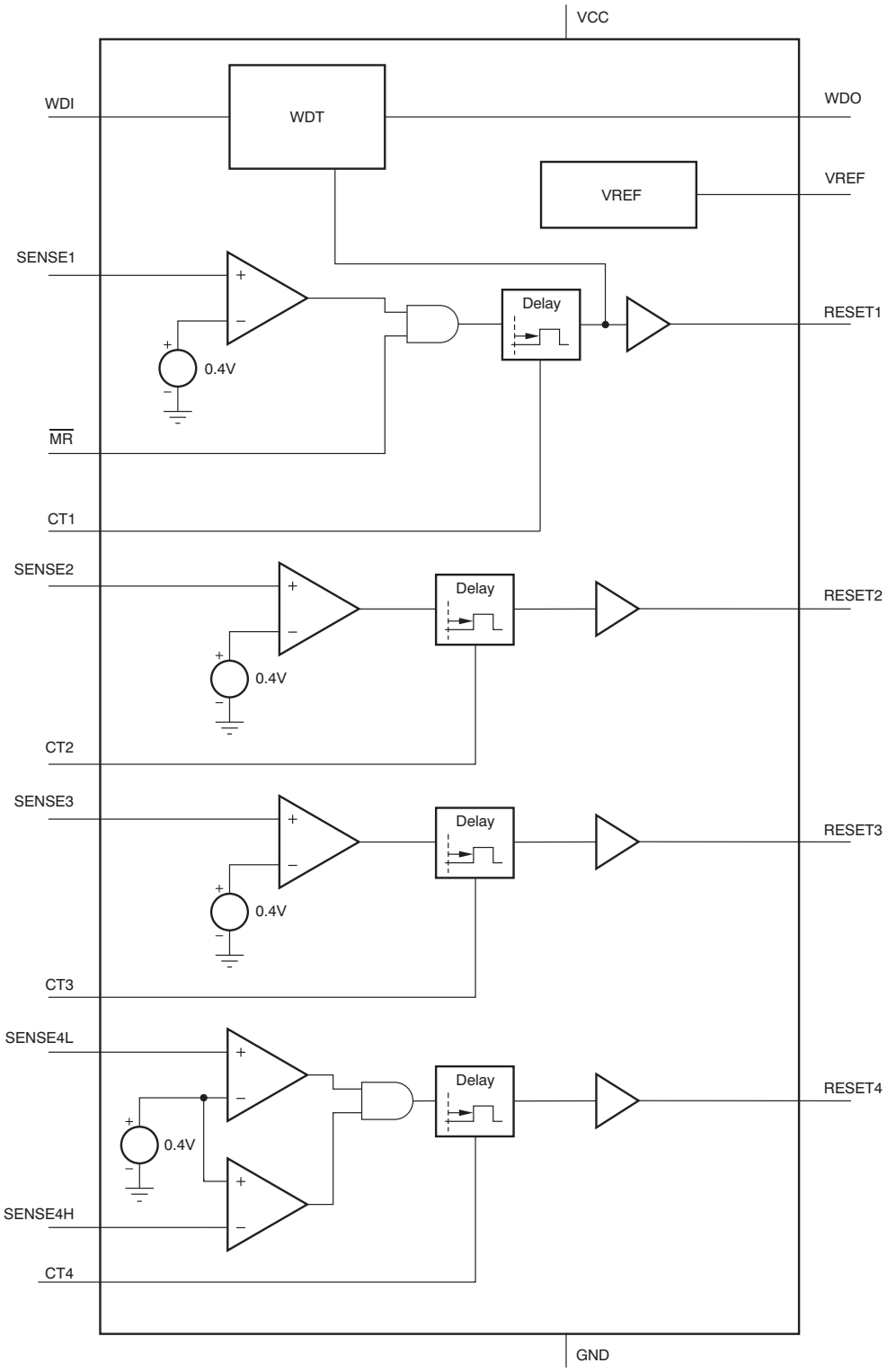

Figure 4. TPS386060 Block Diagram

TYPICAL CHARACTERISTICS

At T_A = +25°C, and V_{CC} = 3.3V, with all four options (TPS386000, TPS386020, TPS386040, and TPS386060) having the same characteristics, unless otherwise noted.

TPS386040
SUPPLY CURRENT vs SUPPLY VOLTAGE

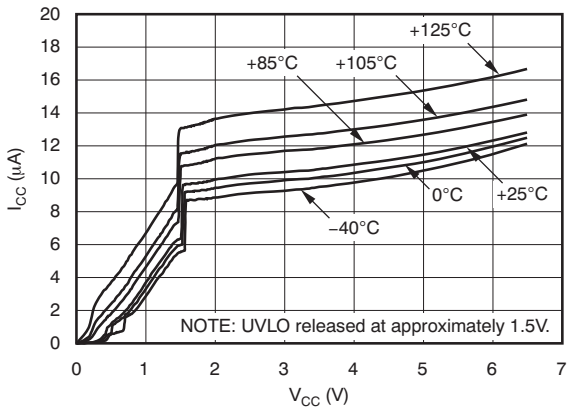

Figure 5.

TPS386040
$\overline{\text{RESETn}}$ TIMEOUT PERIOD vs CTn

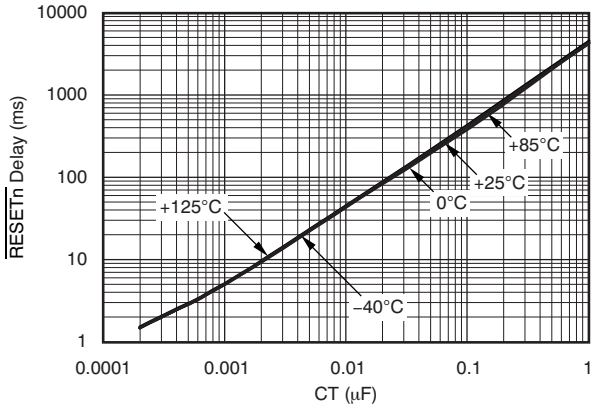

Figure 6.

TPS386040 (CTn = Open)
$\overline{\text{RESETn}}$ TIMEOUT PERIOD vs TEMPERATURE

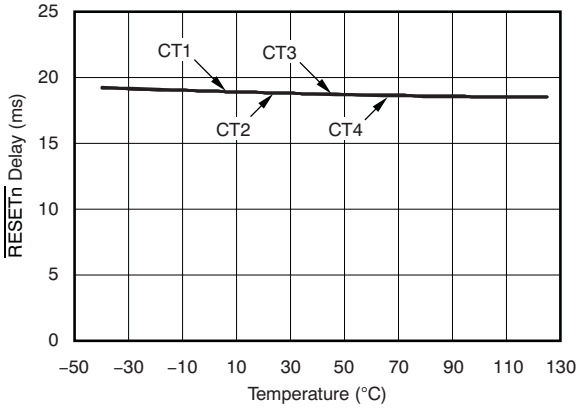

Figure 7.

TPS386040 (CTn = V_{CC})
$\overline{\text{RESETn}}$ TIMEOUT PERIOD vs TEMPERATURE

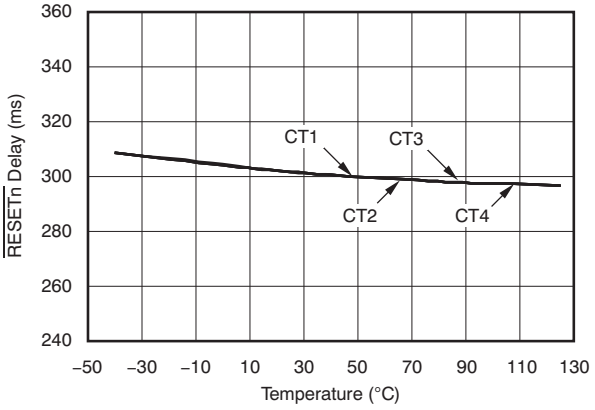

Figure 8.

TPS386040 (CTn = 0.1µF)
$\overline{\text{RESETn}}$ TIMEOUT PERIOD vs TEMPERATURE

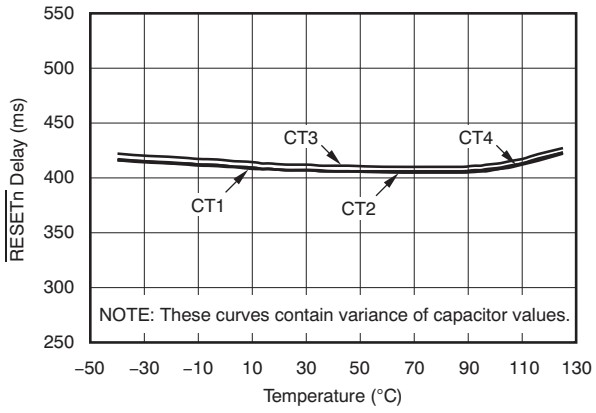

Figure 9.

TPS386040
$\overline{\text{WDO}}$ TIMEOUT PERIOD vs TEMPERATURE

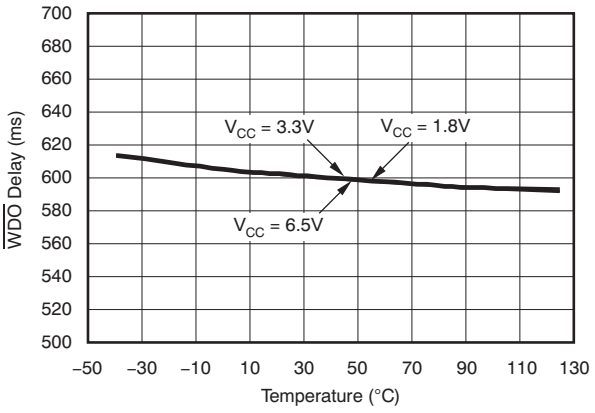

Figure 10.

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TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, and V_{CC} = 3.3V, with all four options (TPS386000, TPS386020, TPS386040, and TPS386060) having the same characteristics, unless otherwise noted.

TPS386040
SENSEn MINIMUM PULSE WIDTH vs SENSEn THRESHOLD OVERDRIVE VOLTAGE

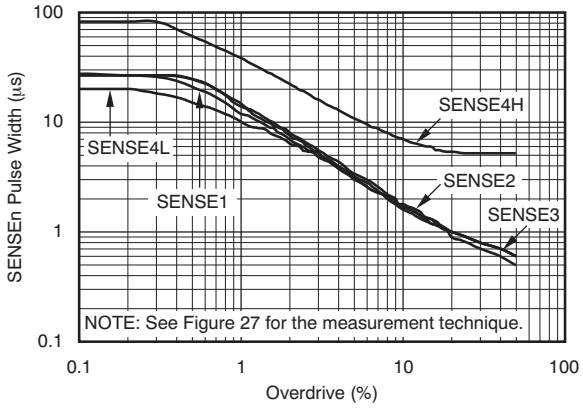

Figure 11.

TPS386040
SENSE1 THRESHOLD VOLTAGE vs TEMPERATURE

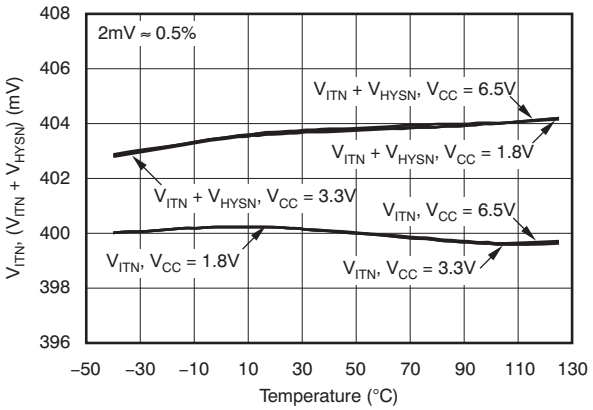

Figure 12.

TPS386040
SENSE2 THRESHOLD VOLTAGE vs TEMPERATURE

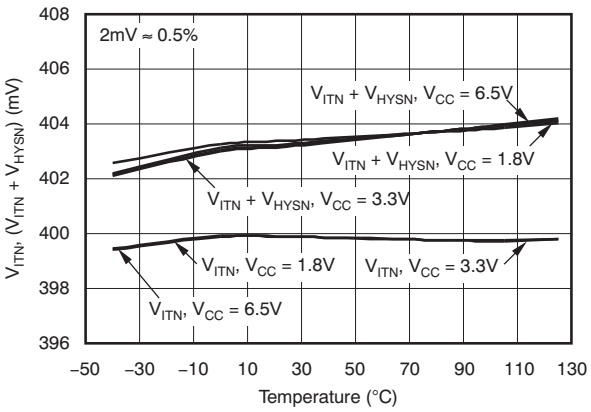

Figure 13.

TPS386040
SENSE3 THRESHOLD VOLTAGE vs TEMPERATURE

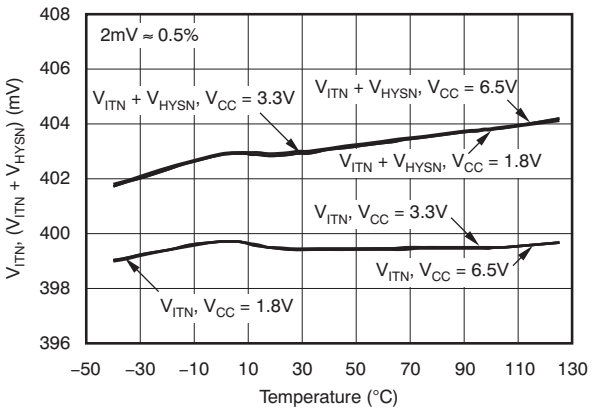

Figure 14.

TPS386040
SENSE4L THRESHOLD VOLTAGE vs TEMPERATURE

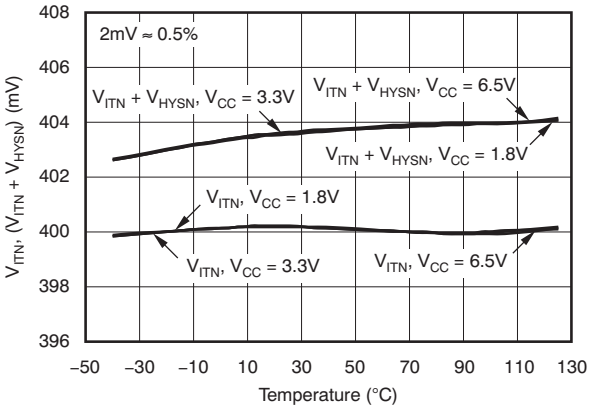

Figure 15.

TPS386040
SENSE4H THRESHOLD VOLTAGE vs TEMPERATURE

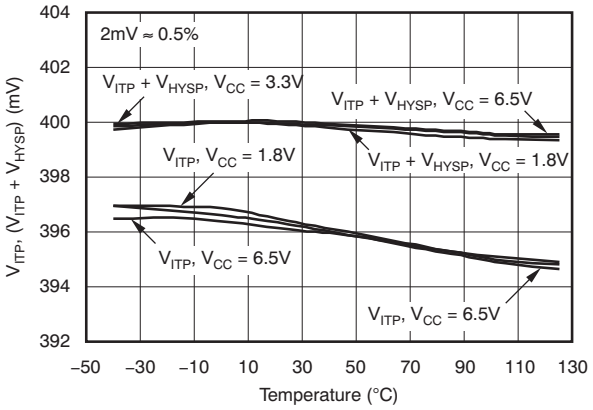

Figure 16.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, and V_{CC} = 3.3V, with all four options (TPS386000, TPS386020, TPS386040, and TPS386060) having the same characteristics, unless otherwise noted.

OUTPUT VOLTAGE LOW vs OUTPUT CURRENT

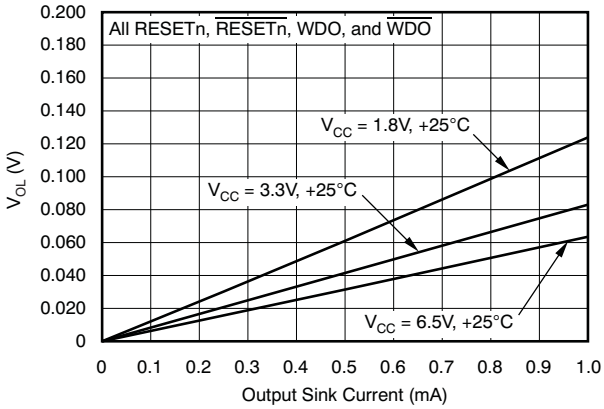

Figure 17.

OUTPUT VOLTAGE LOW AT 1mA vs TEMPERATURE

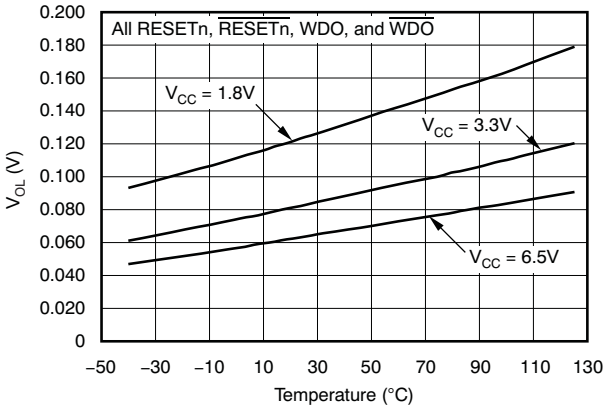

Figure 18.

OUTPUT VOLTAGE HIGH vs OUTPUT CURRENT

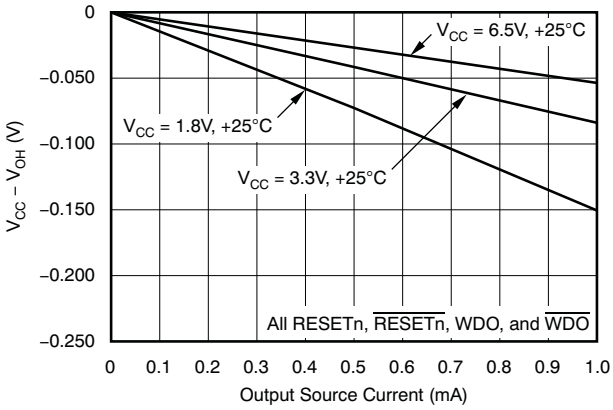

Figure 19.

OUTPUT VOLTAGE HIGH AT 1mA vs TEMPERATURE

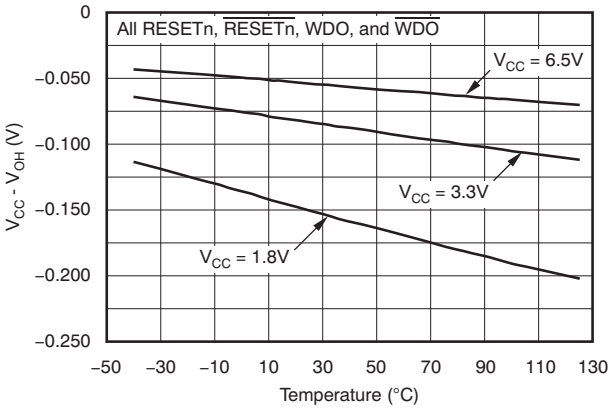

Figure 20.

TPS386040
V_{REF} OUTPUT LOAD REGULATION (V_{CC} = 1.8V)

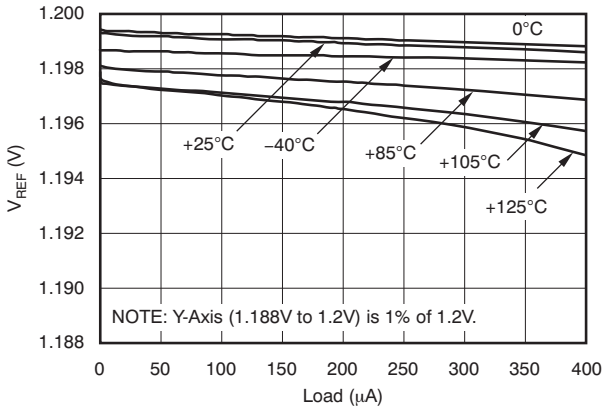

Figure 21.

TPS386040
V_{REF} OUTPUT LOAD REGULATION (V_{CC} = 3.3V)

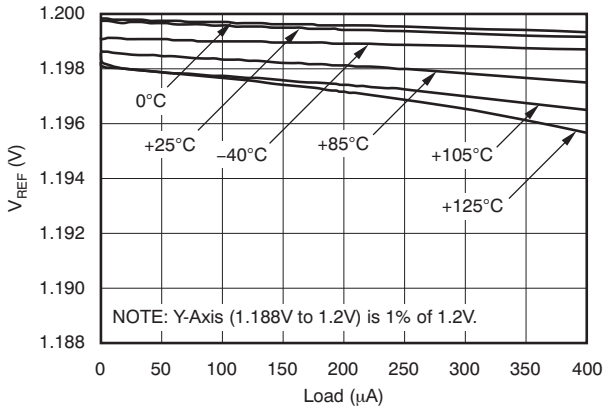

Figure 22.

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TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, and V_{CC} = 3.3V, with all four options (TPS386000, TPS386020, TPS386040, and TPS386060) having the same characteristics, unless otherwise noted.

TPS386040
V_{REF} OUTPUT LOAD REGULATION (V_{CC} = 6.5V)

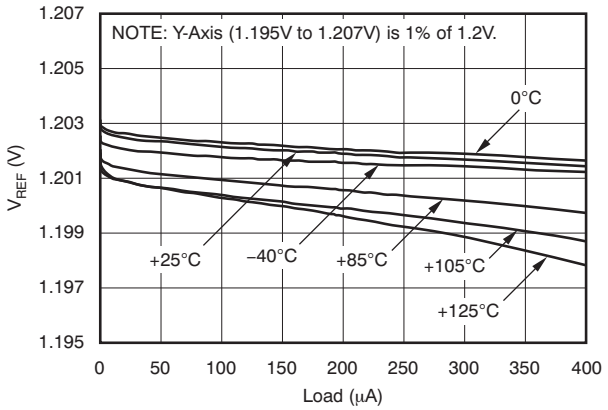


Figure 23.

TPS386040
V_{REF} AT 0µA vs TEMPERATURE

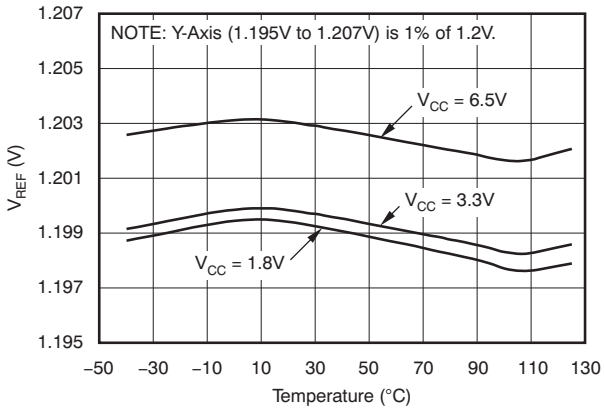


Figure 24.

TPS386040
CT1 TO CT4 PIN CHARGING CURRENT vs TEMPERATURE OVER CT PIN VOLTAGE

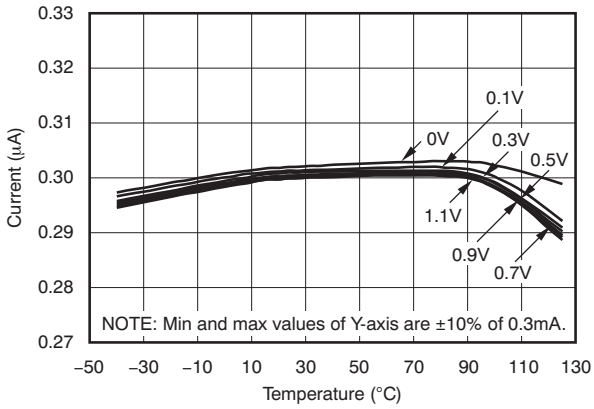
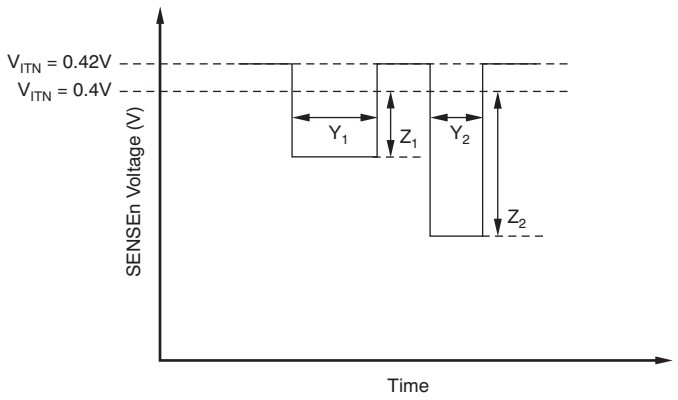


Figure 25.

PARAMETRIC MEASUREMENT INFORMATION

TEST CIRCUIT



$$X_1 = \frac{Z_1}{0.4} \times 100\ (\%)$$

$$X_2 = \frac{Z_2}{0.4} \times 100\ (\%)$$

X_1 and X_2 are overdrive (%) values calculated from actual SENSEn voltage amplitudes measured as Z_1 and Z_2.
Y_N is the minimum pulse width that gives RESETn or $\overline{\text{RESETn}}$ transition.
Greater Z_N produces shorter Y_N.

For SENSE4H, this graph should be inverted 180 degrees on the voltage axis.

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GENERAL DESCRIPTION

The TPS3860x0 multi-channel supervisory device family combines four complete SVS function sets into one IC, along with a watchdog timer, a window comparator, and negative voltage sensing. The design of each SVS channel is based on the single-channel supervisory device series, TPS3808. The TPS3860x0 is designed to assert $\overline{\text{RESET}}$n or RESETn signals, as shown in Table 1, Table 2, Table 3, and Table 4. The $\overline{\text{RESET}}$n or RESETn outputs remain asserted during a user-configurable delay time after the event of reset release (see the Reset Delay Time section). Each SENSEm (m = 1, 2, 3, 4L) pin can be set to any voltage threshold above 0.4V using an external resistor divider. The SENSE4H pin can be used for any overvoltage detection greater than 0.4V, or for negative voltage detection using an external resistor divider (see the *Sensing Voltage Less Than 0.4V* section). A broad range of voltage threshold and reset delay time adjustments can be supported, allowing these devices to be used in a wide array of applications.

Table 1. SVS-1 Truth Table

CONDITION		OUTPUT		STATUS
		TPS386000 TPS386040	TPS386020 TPS386060	
$\overline{\text{MR}}$ = Low	SENSE1 < V_{ITN}	$\overline{\text{RESET1}}$ = Low	RESET1 = High	Reset asserted
$\overline{\text{MR}}$ = Low	SENSE1 > V_{ITN}	$\overline{\text{RESET1}}$ = Low	RESET1 = High	Reset asserted
$\overline{\text{MR}}$ = High	SENSE1 < V_{ITN}	$\overline{\text{RESET1}}$ = Low	RESET1 = High	Reset asserted
$\overline{\text{MR}}$ = High	SENSE1 > V_{ITN}	$\overline{\text{RESET1}}$ = High	RESET1 = Low	**Reset released after delay**

Table 2. SVS-2 Truth Table

CONDITION	OUTPUT		STATUS
	TPS386000 TPS386040	TPS386020 TPS386060	
SENSE2 < V_{ITN}	$\overline{\text{RESET2}}$ = Low	RESET2 = High	Reset asserted
SENSE2 > V_{ITN}	$\overline{\text{RESET2}}$ = High	RESET2 = Low	**Reset released after delay**

Table 3. SVS-3 Truth Table

CONDITION	OUTPUT		STATUS
	TPS386000 TPS386040	TPS386020 TPS386060	
SENSE3 < V_{ITN}	$\overline{\text{RESET3}}$ = Low	RESET3 = High	Reset asserted
SENSE3 > V_{ITN}	$\overline{\text{RESET3}}$ = High	RESET3 = Low	**Reset released after delay**

Table 4. SVS-4 Truth Table

CONDITION		OUTPUT		STATUS
		TPS386000 TPS386040	TPS386020 TPS386060	
SENSE4L < V_{ITN}	SENSE4H > V_{ITP}	$\overline{\text{RESET4}}$ = Low	RESET4 = High	Reset asserted
SENSE4L < V_{ITN}	SENSE4H < V_{ITP}	$\overline{\text{RESET4}}$ = Low	RESET4 = High	Reset asserted
SENSE4L > V_{ITN}	SENSE4H > V_{ITP}	$\overline{\text{RESET4}}$ = Low	RESET4 = High	Reset asserted
SENSE4L > V_{ITN}	SENSE4H < V_{ITP}	$\overline{\text{RESET4}}$ = High	RESET4 = Low	**Reset released after delay**

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Table 5. Watchdog Timer (WDT) Truth Table

CONDITION				OUTPUT		
$\overline{\text{WDO}}$	WDO	$\overline{\text{RESET1}}$ OR RESET1	WDI PULSE INPUT	TPS386000 TPS386040	TPS386020 TPS386060	STATUS
Low	High	Asserted	Toggling	$\overline{\text{WDO}}$ = low	WDO = high	Remains in WDT timeout
Low	High	Asserted	610ms after last WDI↑ or WDI↓	$\overline{\text{WDO}}$ = low	WDO = high	Remains in WDT timeout
Low	High	Released	Toggling	$\overline{\text{WDO}}$ = low	WDO = high	Remains in WDT timeout
Low	High	Released	610ms after last WDI↑ or WDI↓	$\overline{\text{WDO}}$ = low	WDO = high	Remains in WDT timeout
High	Low	Asserted	Toggling	$\overline{\text{WDO}}$ = high	WDO = low	Normal operation
High	Low	Asserted	610ms after last WDI↑ or WDI↓	$\overline{\text{WDO}}$ = high	WDO = low	Normal operation
High	Low	Released	Toggling	$\overline{\text{WDO}}$ = high	WDO = low	Normal operation
High	Low	Released	610ms after last WDI↑ or WDI↓	$\overline{\text{WDO}}$ = low	WDO = high	Enters WDT timeout

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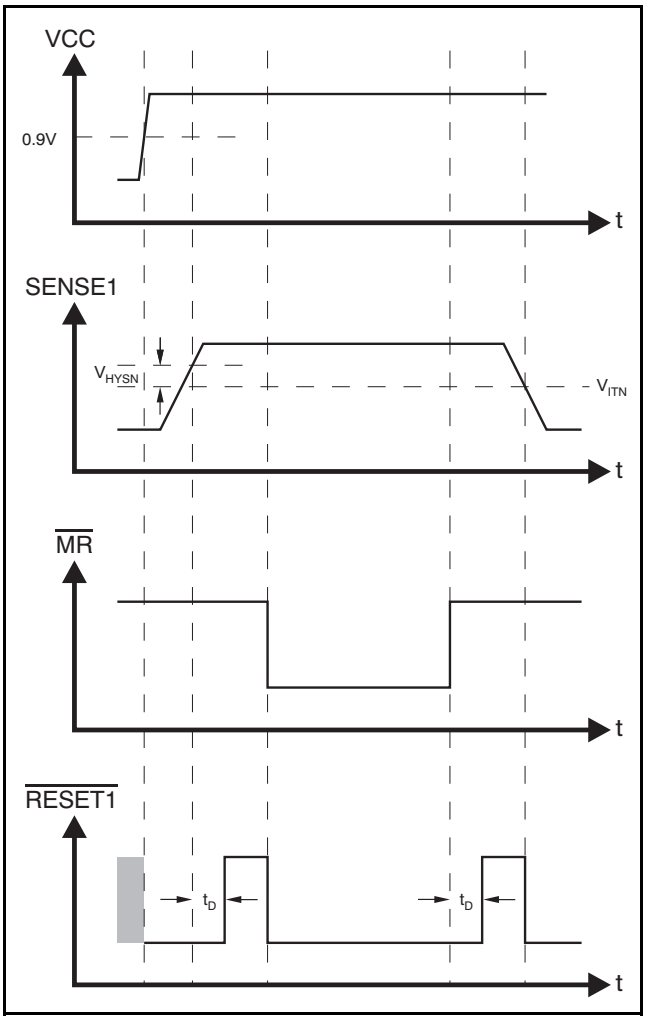
RESET OUTPUT

In a typical TPS3860x0 application, $\overline{\text{RESETn}}$ or RESETn outputs are connected to the reset input of a processor (DSP, CPU, FPGA, ASIC, etc.), or connected to the enable input of a voltage regulator (DC-DC, LDO, etc.)

The TPS386000 and TPS386020 provide open-drain reset outputs. Pull-up resistors must be used to hold these lines high when $\overline{\text{RESETn}}$ is not asserted, or when RESETn is asserted. By connecting pull-up resistors to the proper voltage rails (up to 6.5V), $\overline{\text{RESETn}}$ or RESETn output nodes can be connected to the other devices at the correct interface voltage levels. The pull-up resistor should be no smaller than 10kΩ because of the safe operation of the output transistors. By using wired-OR logic, any combination of $\overline{\text{RESETn}}$ can be merged into one logic signal.

The TPS386040 and TPS386060 provide push-pull reset outputs. The logic high level of the outputs is determined by the VCC voltage. With this configuration, pull-up resistors are not required and some board area can be saved. However, all the interface logic levels should be examined. All $\overline{\text{RESETn}}$ or RESETn connections must be compatible with the VCC logic level.

The $\overline{\text{RESETn}}$ or RESETn outputs are defined for VCC voltage higher than 0.9V. To ensure that the target processor(s) are properly reset, the VCC supply input should be fed by the available power rail as early as possible in application circuits. Table 1, Table 2, Table 3, and Table 4 are truth tables that describe how the outputs are asserted or released. Figure 26, Figure 27, Figure 28, and Figure 29 show the SVS-n timing diagrams. When the condition(s) are met, the device changes the state of SVS-n from asserted to released after a user-configurable delay time. However, the transitions from released-state to asserted-state are performed almost immediately with minimal propagation delay. Figure 28 describes relationship between threshold voltages (V_{ITN} and V_{HYSN}) and SENSEm voltage; and all SVS-1, SVS-2, SVS-3, and SVS-4 have the same behavior of Figure 28.



NOTE: The TPS386000 or TPS386040 is shown here using $\overline{\text{RESETn}}$. The TPS386020 and TPS386060 use RESETn; therefore, the diagram of $\overline{\text{RESETn}}$ should be read as RESETn with the opposite polarity.

Figure 26. SVS-1 Timing Diagram

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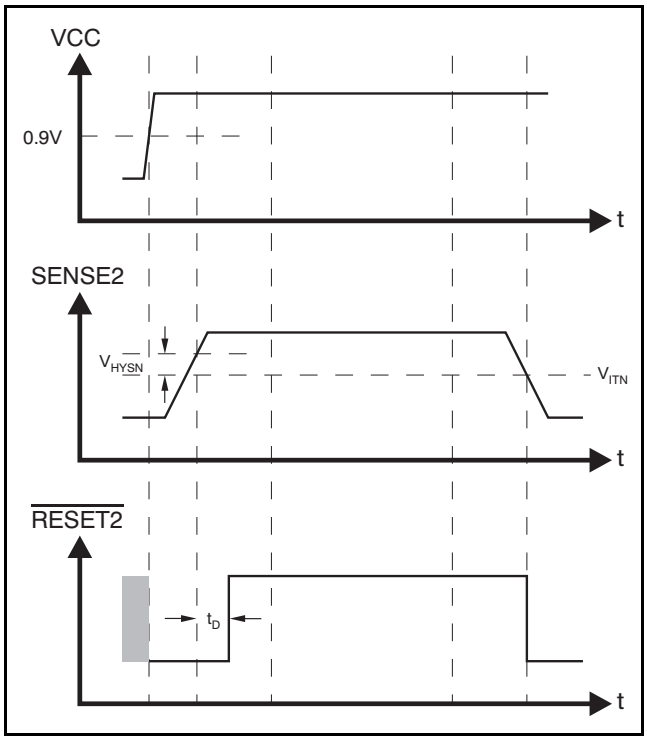
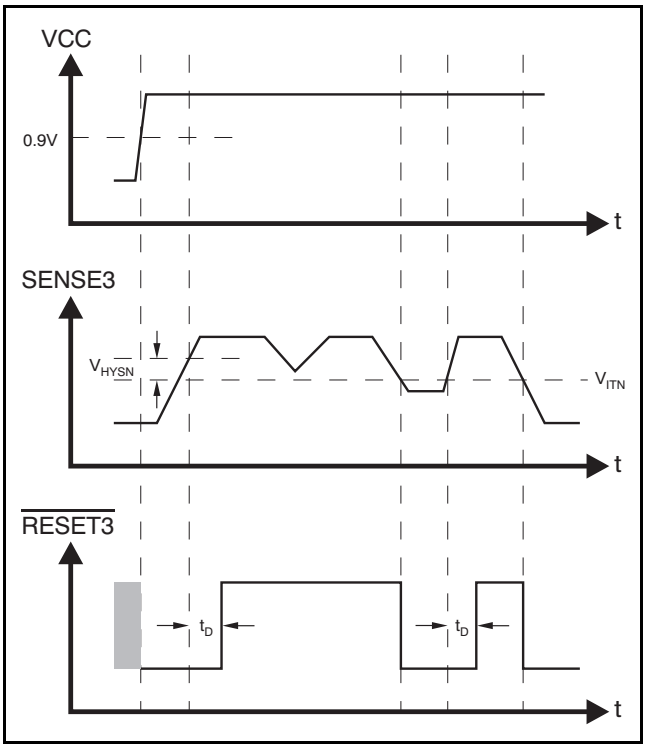


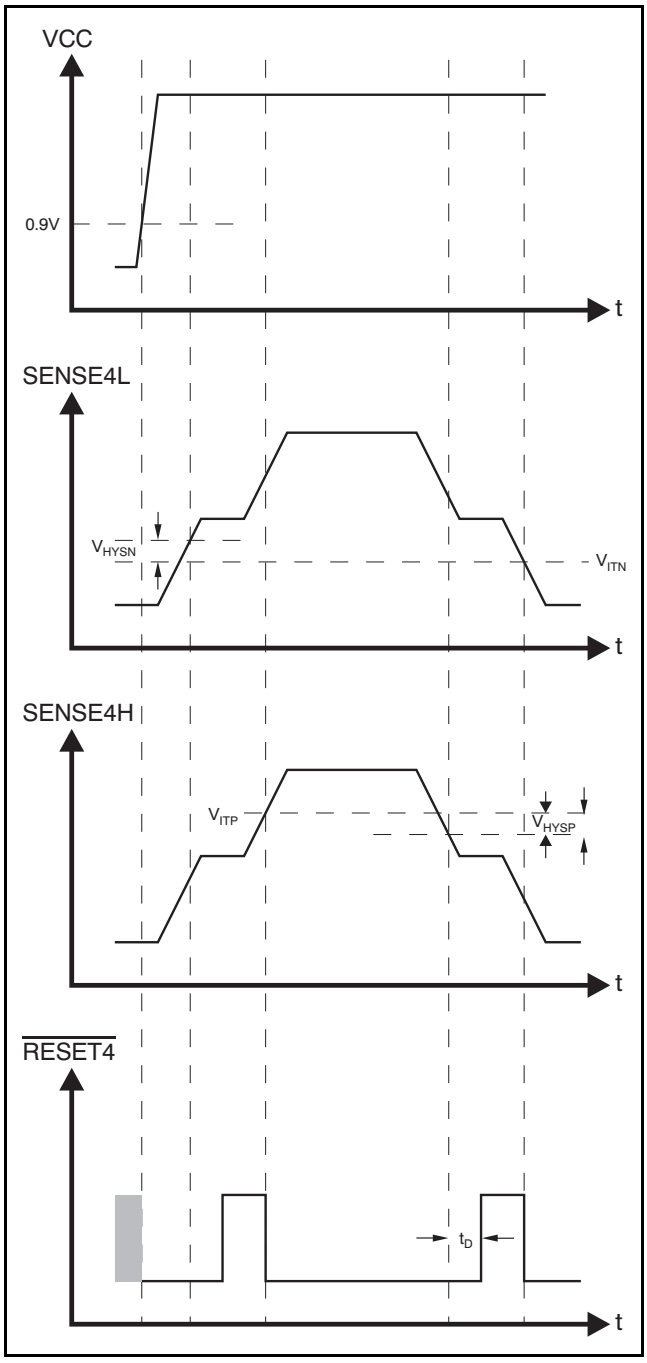
NOTE: The TPS386000 or TPS386040 is shown here using $\overline{\text{RESETn}}$. The TPS386020 and TPS386060 use RESETn; therefore, the diagram of $\overline{\text{RESETn}}$ should be read as RESETn with the opposite polarity.

Figure 27. SVS-2 Timing Diagram



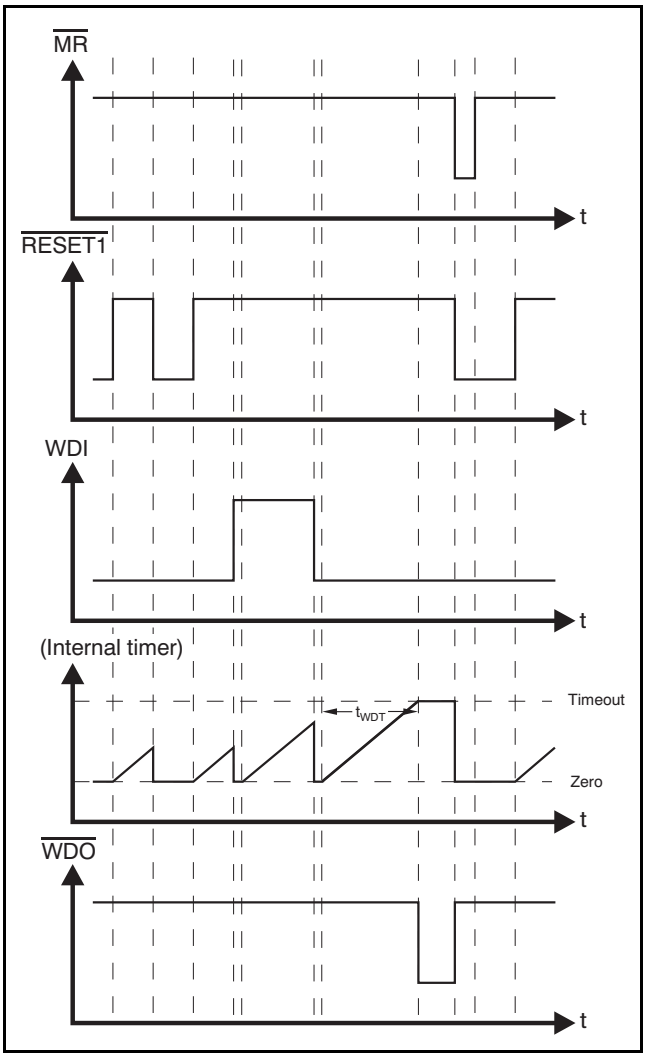
NOTE: The TPS386000 or TPS386040 is shown here using $\overline{\text{RESETn}}$. The TPS386020 and TPS386060 use RESETn; therefore, the diagram of $\overline{\text{RESETn}}$ should be read as RESETn with the opposite polarity.

Figure 28. SVS-3 Timing Diagram



NOTE: The TPS386000 or TPS386040 is shown here using $\overline{\text{RESETn}}$. The TPS386020 and TPS386060 use RESETn; therefore, the diagram of $\overline{\text{RESETn}}$ should be read as RESETn with the opposite polarity.

Figure 29. SVS-4 Timing Diagram



NOTE: The TPS386000 or TPS386040 is shown here using $\overline{\text{RESETn}}$ and $\overline{\text{WDO}}$. The TPS386020 and TPS386060 use RESETn and WDO; therefore, the diagrams of $\overline{\text{RESETn}}$ and $\overline{\text{WDO}}$ should be read as RESETn and WDO with the opposite polarities.

Figure 30. WDT Timing Diagram

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SENSE INPUT

The SENSEm inputs are pins that allow any system voltages to be monitored. If the voltage at the SENSE1, SENSE2, SENSE3, or SENSE4L pins drops below V_{ITN}, then the corresponding reset outputs are asserted. If the voltage at the SENSE4H pin exceeds V_{ITP}, then $\overline{RESET4}$ or RESET4 is asserted. The comparators have a built-in hysteresis to ensure smooth reset output assertions and deassertions. Although not required in most cases, for extremely noise applications, it is good analog design practice to place a 1nF to 10nF bypass capacitor at the SENSEm input in order to reduce sensitivity to transients, layout parasitics, and interference between power rails monitored by this device. A typical connection of resistor dividers are shown in Figure 31. All the SENSEm pins can be used to monitor voltage rails down to 0.4V. Threshold voltages can be calculated by following equations:

$$VCC1_target = (1 + R_{S1H}/R_{S1L}) \times 0.4\ (V) \quad (1)$$

$$VCC2_target = (1 + R_{S2H}/R_{S2L}) \times 0.4\ (V) \quad (2)$$

$$VCC3_target = (1 + R_{S3H}/R_{S3L}) \times 0.4\ (V) \quad (3)$$

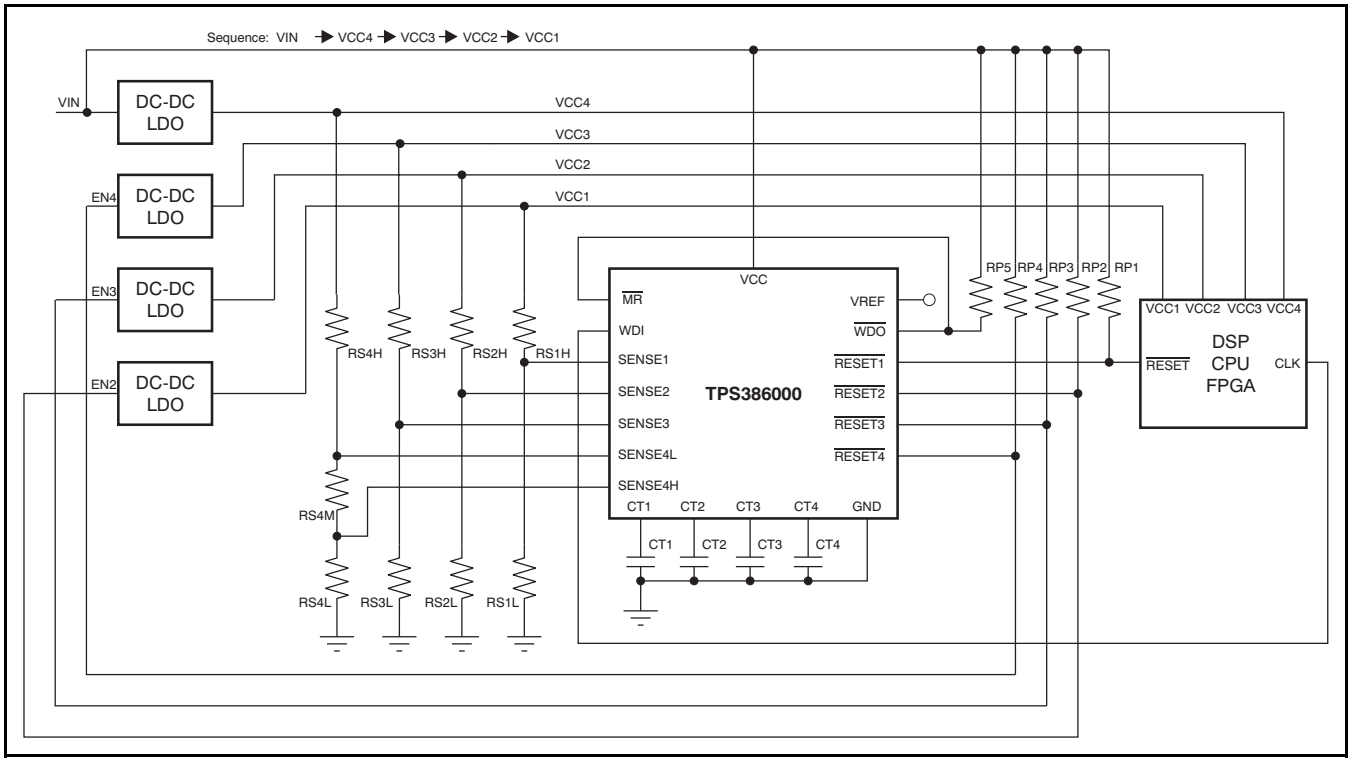

Figure 31. Typical Application Circuit

WINDOW COMPARATOR

The comparator at the SENSE4H pin has the opposite comparison polarity to the other SENSEm pins. In the configuration shown in Figure 32, this comparator monitors overvoltage of the VCC4 node; combined with the comparator at SENSE4L, SVS-4 forms a window comparator.

$$VCC4_target1 = \{1+ R_{S4H}/(R_{S4M} + R_{S4L})\} \times 0.4\ (V) \quad (4)$$

$$VCC4_target2 = \{1+ (R_{S4H} + R_{S4M})/R_{S4L}\} \times 0.4\ (V) \quad (5)$$

Where VCC4_target1 is the undervoltage threshold, and VCC4_target2 is the overvoltage threshold.

SENSING VOLTAGE LESS THAN 0.4V

By using voltage reference output VREF, the SVS-4 comparator can monitor negative voltage or positive voltage lower than 0.4V. Figure 33 shows this usage in an application circuit. SVS-4 monitors the positive and negative voltage power rail (for example, +15V and –15V supply to an op amp) and the $\overline{\text{RESET4}}$ or RESET4 output status continues to be as described in Table 4. Note that R_{S42H} is located at higher voltage position than R_{S42L}. The threshold voltage calculations are shown in the following equations:

$$VCC41_target = (1+R_{S41H}/R_{S41L}) \times 0.4\ (V) \quad (6)$$

$$VCC42_target = (1+R_{S42L}/R_{S42H}) \times 0.4 - R_{S42L}/R_{S42H} \times V_{REF} \quad (7)$$

$$= 0.4 - (R_{S42L}/R_{S42H} \times 0.8\ (V)) \quad (8)$$

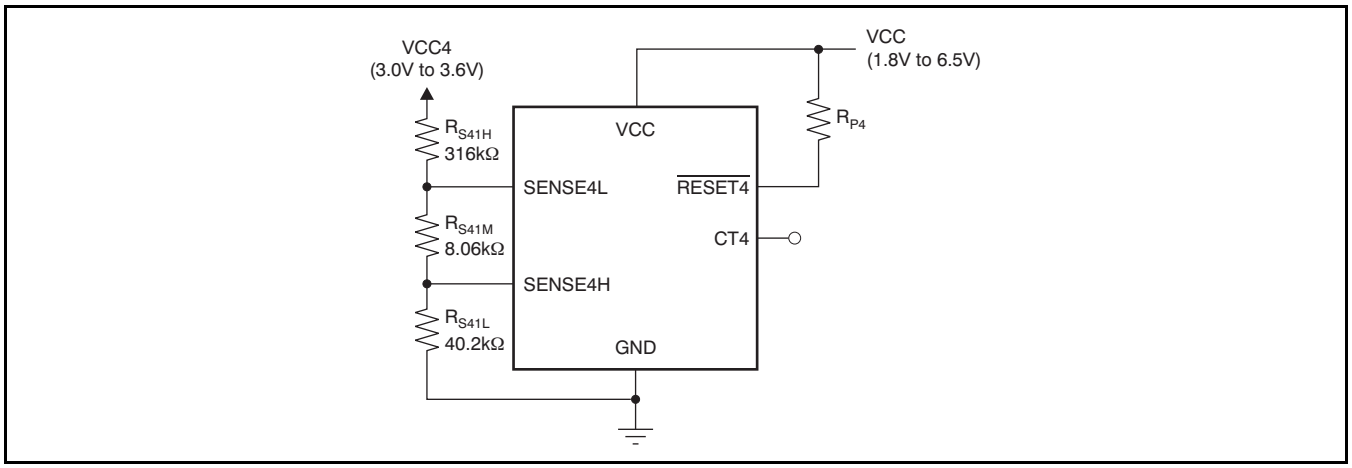

Figure 32. SVS-4: Window Comparator

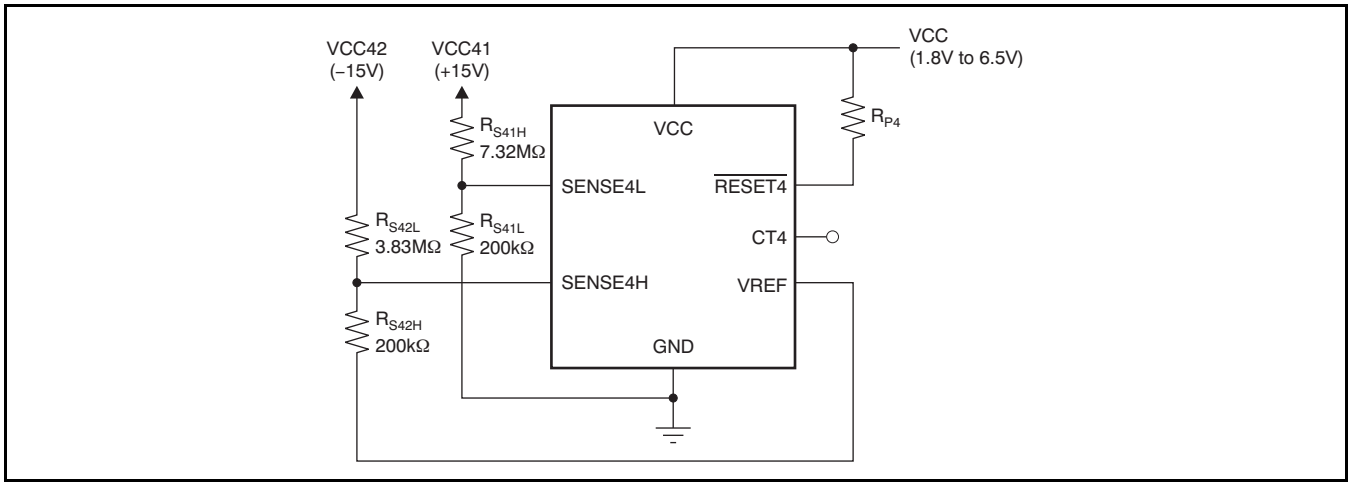

Figure 33. SVS4: Negative Voltage Sensing

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RESET DELAY TIME

Each of the SVS-n channels can be configured independently in one of three modes. Table 6 describes the delay time settings.

Table 6. Delay Timing Selection

CTn CONNECTION	DELAY TIME
Pull-up to VCC	300ms (typ)
Open	20 ms (typ)
Capacitor to GND	Programmable

To select the 300ms fixed delay time, the CTn pin should be pulled up to VCC using a resistor from 40kΩ to 200kΩ. Please note that there is a pulldown transistor from CTn to GND that turns on every time the device powers on to determine and confirm CTn pin status; therefore, a direct connection of CTn to VCC causes a large current flow. To select the 20ms fixed delay time, the CTn pin should be left open. To program a user-defined adjustable delay time, an external capacitor must be connected between CTn and GND. The adjustable delay time can be calculated by the following equation:

$$C_{CT}\ (nF) = [t_{DELAY}\ (ms) - 0.5(ms)] \times 0.242 \quad (9)$$

Using this equation, a delay time can be set to between 1.4ms to 10s. The external capacitor should be greater than 220pF (nominal) so that the TPS3860x0 can distinguish it from an open CT pin. The reset delay time is determined by the time it takes an on-chip, precision 300nA current source to charge the external capacitor to 1.24V. When the RESETn or RESETn outputs are asserted, the corresponding capacitors are discharged. When the condition to release RESETn or RESETn occurs, the internal current sources are enabled and begin to charge the external capacitors. When the CTn voltage on a capacitor reaches 1.24V, the corresponding RESETn or RESETn pins are released. Note that a low leakage type capacitor (such as ceramic) should be used, and that stray capacitance around this pin may cause errors in the reset delay time.

MANUAL RESET

The manual reset ($\overline{MR}$) input allows external logic signal from other processors, logic circuits, and/or discrete sensors to initiate a device reset. Because $\overline{MR}$ is connected to SVS-1, the $\overline{RESET1}$ or RESET1 pin is intended to be connected to processor(s) as a primary reset source. A logic low at $\overline{MR}$ causes $\overline{RESET1}$ or RESET1 to assert. After $\overline{MR}$ returns to a logic high and SENSE1 is above its reset threshold, $\overline{RESET1}$ or RESET1 is released after the user-configured reset delay time. Note that unlike the TPS3808 series, the TPS3860x0 does not integrate an internal pull-up resistor between $\overline{MR}$ and VCC.

To control the $\overline{MR}$ function from more than one logic signal, the logic signals can be combined by wired-OR into the $\overline{MR}$ pin using multiple NMOS transistors and one pull-up resistor.

WATCHDOG TIMER

The TPS3860x0 provides a watchdog timer with a dedicated watchdog error output, $\overline{WDO}$ or WDO. The $\overline{WDO}$ or WDO output enables application board designers to easily detect and resolve the hang-up status of a processor. As with $\overline{MR}$, the watchdog timer function of the device is also tied to SVS-1. Figure 30 shows the timing diagram of the WDT function. Once $\overline{RESET1}$ or RESET1 is released, the internal watchdog timer starts its countdown. Inputting a logic level transition at WDI resets the internal timer count and the timer restarts the countdown. If the TPS3860x0 fails to receive any WDI rising or falling edge within the WDT period, the WDT times out and asserts $\overline{WDO}$ or WDO. After $\overline{WDO}$ or WDO is asserted, the device holds the status with the internal latch circuit. To clear this timeout status, a reset assertion of $\overline{RESET1}$ or RESET is required. That is, a negative pulse to $\overline{MR}$, a SENSE1 voltage less than V_{ITN}, or a VCC power-down is required.

To reset the processor by WDT timeout, $\overline{WDO}$ can be combined with $\overline{RESET1}$ by using the wired-OR with the TPS386000 option.

For legacy applications where the watchdog timer timeout causes $\overline{RESET1}$ to assert, connect $\overline{WDO}$ to $\overline{MR}$; see Figure 31 for the connections and see Figure 34 and Figure 35 for the timing diagram. This legacy support configuration is available with the TPS386000 and TPS386040.

IMMUNITY TO SENSEn VOLTAGE TRANSIENTS

The TPS3860x0 is relatively immune to short negative transients on the SENSEn pin. Sensitivity to transients depends on threshold overdrive, as shown in the typical performance graph *TPS386040 SENSEn Minimum Pulse Width vs SENSEn Threshold Overdrive Voltage* (Figure 11).

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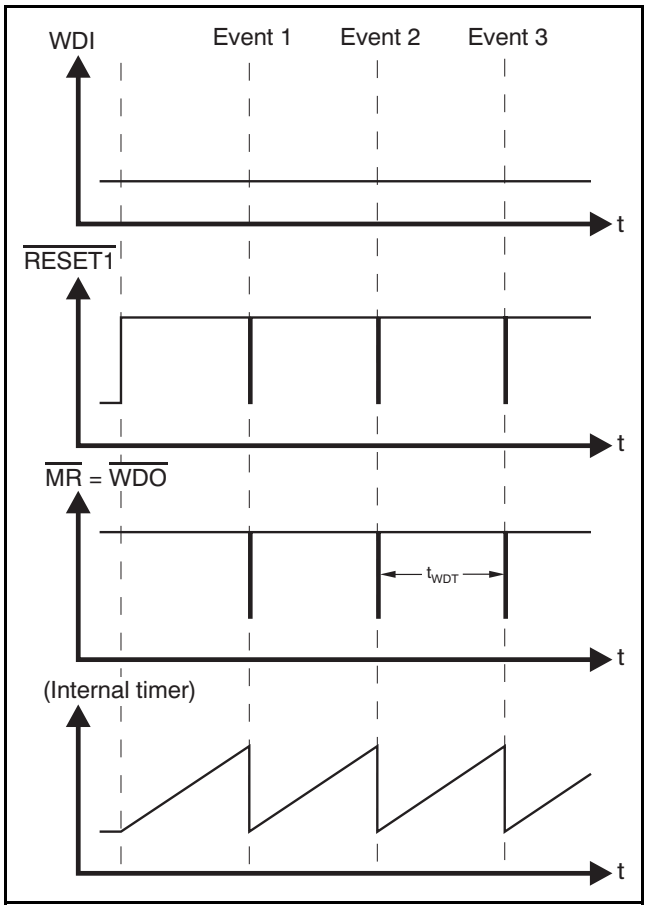
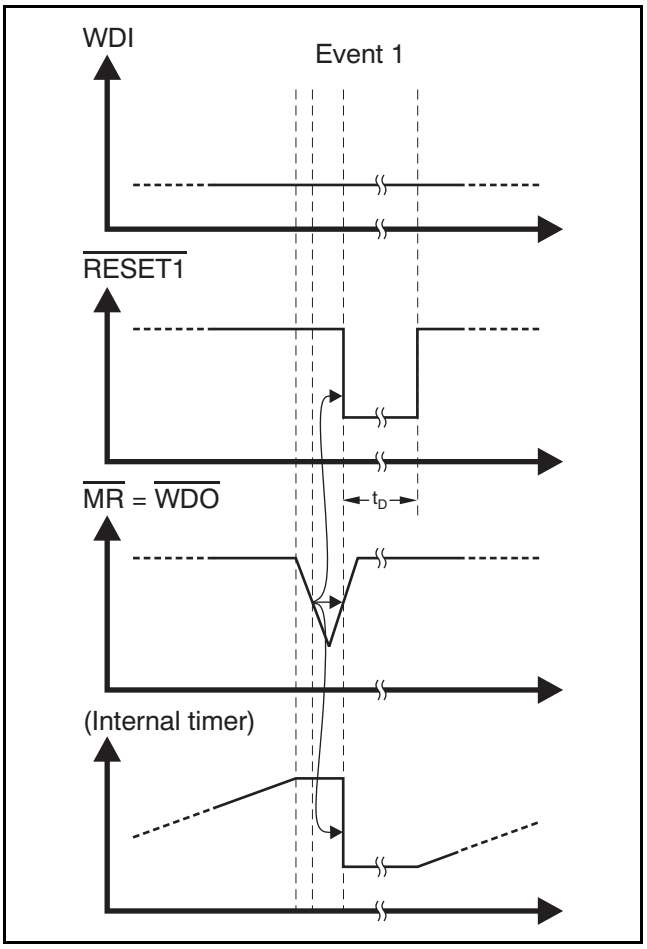


NOTE: This configuration (connecting $\overline{WDO}$ and $\overline{MR}$) is available only with the TPS386000 and TPS386040.

Figure 34. Legacy WDT Configuration Timing Diagram



NOTE: This configuration (connecting $\overline{WDO}$ and $\overline{MR}$) is available only with the TPS386000 and TPS386040.

Figure 35. Enlarged View of Event 1 from Figure 34

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REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (January 2010) to Revision B **Page**

- Changed data sheet title 1
- Changed Features bullets 1
- Changed Applications bullets 1
- Changed first sentence of second paragraph in Description text 1
- Changed low quiescent current value in last paragraph of Description text from 12µA to 11µA 1
- Changed front-page typical application circuit figure 1
- Added sentence to pin 6 description in Pin Assignments table 4
- Changed last sentence of pin 13 description in Pin Assignments table 4
- Added text to first sentence of first paragraph of *General Description* section. 14
- Changed caption for Figure 31 19
- Changed link in *Window Comparator* section to new Figure 32 20
- Deleted typo in Equation 4 and moved Equation 4 to *Window Comparator* section 20
- Deleted typo in Equation 5 and moved Equation 5 to *Window Comparator* section 20
- Changed link in *Sensing Voltage Less Than 0.4V* section to new Figure 33 20
- Added Figure 32 20
- Added Figure 33 20

Changes from Original (September 2009) to Revision A **Page**

- Changed Features to update SVS bullets 1
- Changed first sentence of Description text. 1
- Changed text in *General Description* section regarding SENSE4H pin 14
- Changed title of *Negative Voltage Sensing* section to *Sensing Voltage Less Than 0.4V* 20

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TPS386000RGPR	ACTIVE	QFN	RGP	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TPS386000RGPT	ACTIVE	QFN	RGP	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TPS386040RGPR	ACTIVE	QFN	RGP	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TPS386040RGPT	ACTIVE	QFN	RGP	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TPS386060RGPR	PREVIEW	QFN	RGP	20	3000	TBD	Call TI	Call TI	
TPS386060RGPT	PREVIEW	QFN	RGP	20	250	TBD	Call TI	Call TI	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF TPS386000 :

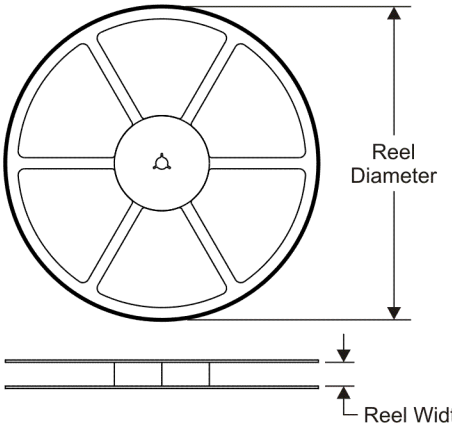
- Automotive: TPS386000-Q1

NOTE: Qualified Version Definitions:

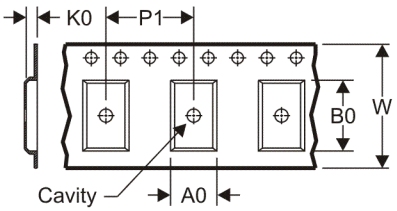
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

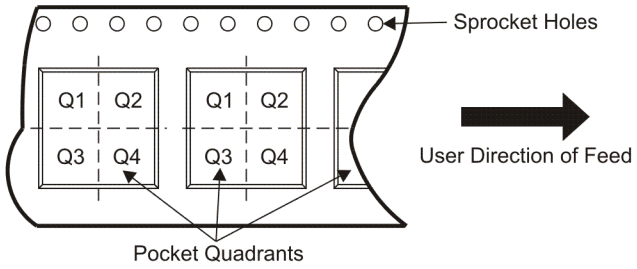


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

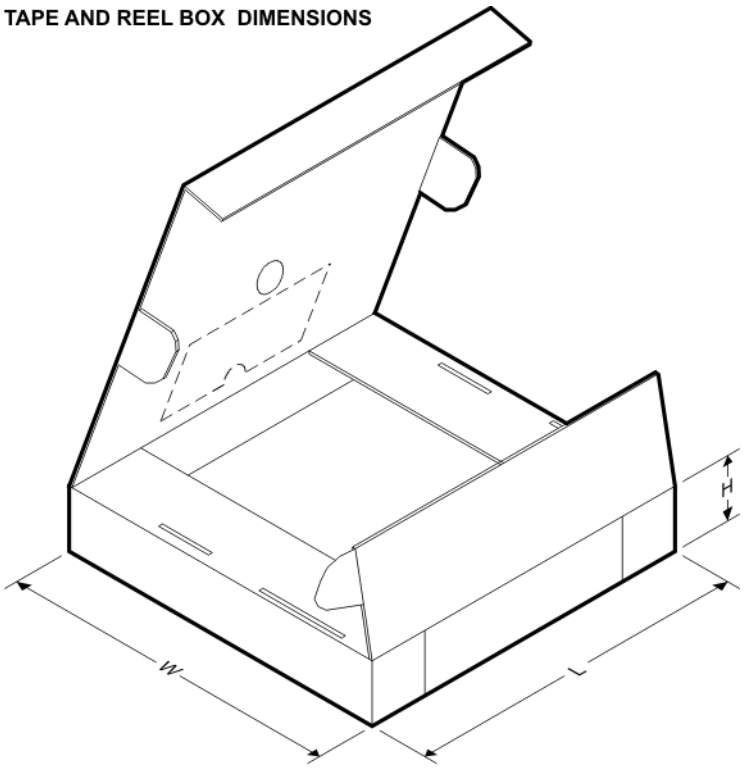
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS386000RGPR	QFN	RGP	20	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS386000RGPT	QFN	RGP	20	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS386040RGPR	QFN	RGP	20	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS386040RGPT	QFN	RGP	20	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

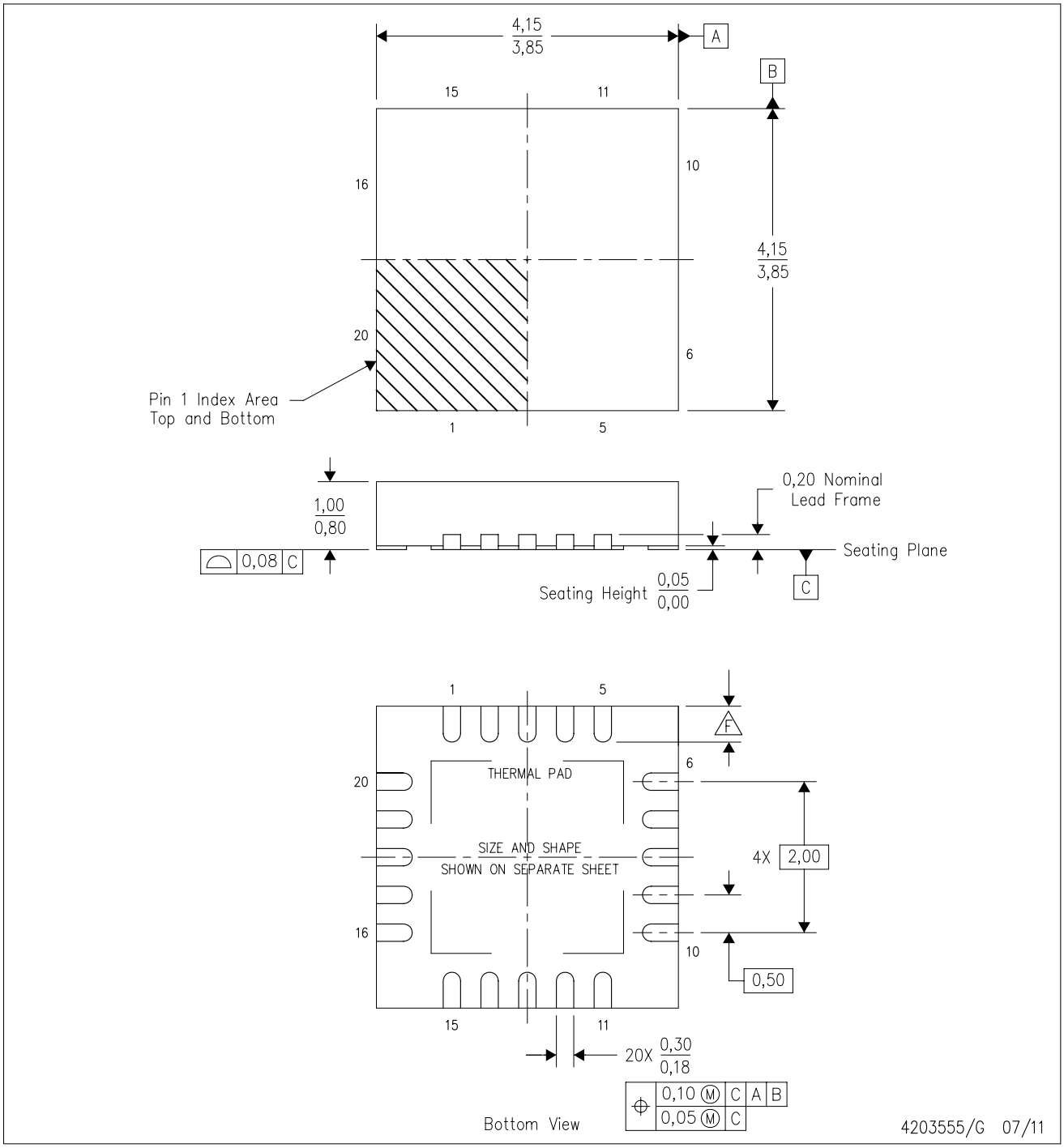
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS386000RGPR	QFN	RGP	20	3000	346.0	346.0	29.0
TPS386000RGPT	QFN	RGP	20	250	190.5	212.7	31.8
TPS386040RGPR	QFN	RGP	20	3000	346.0	346.0	29.0
TPS386040RGPT	QFN	RGP	20	250	190.5	212.7	31.8

RGP (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Check thermal pad mechanical drawing in the product datasheet for nominal lead length dimensions.

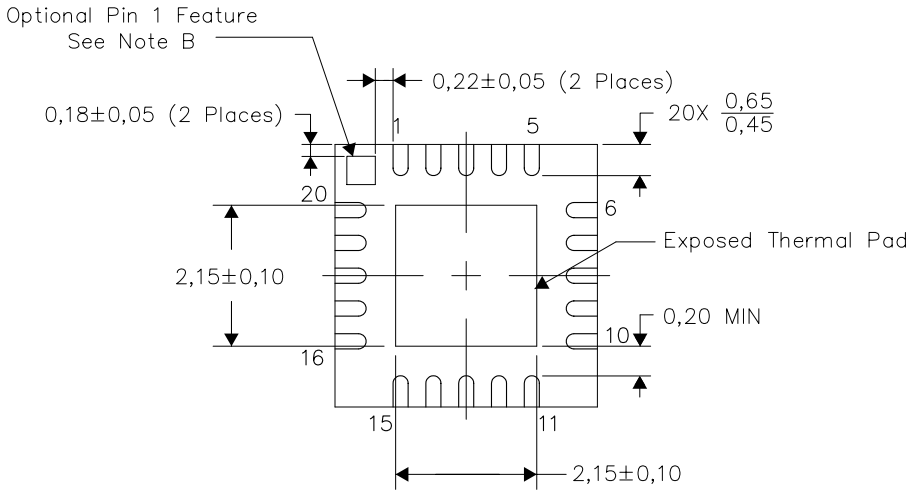
RGP (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

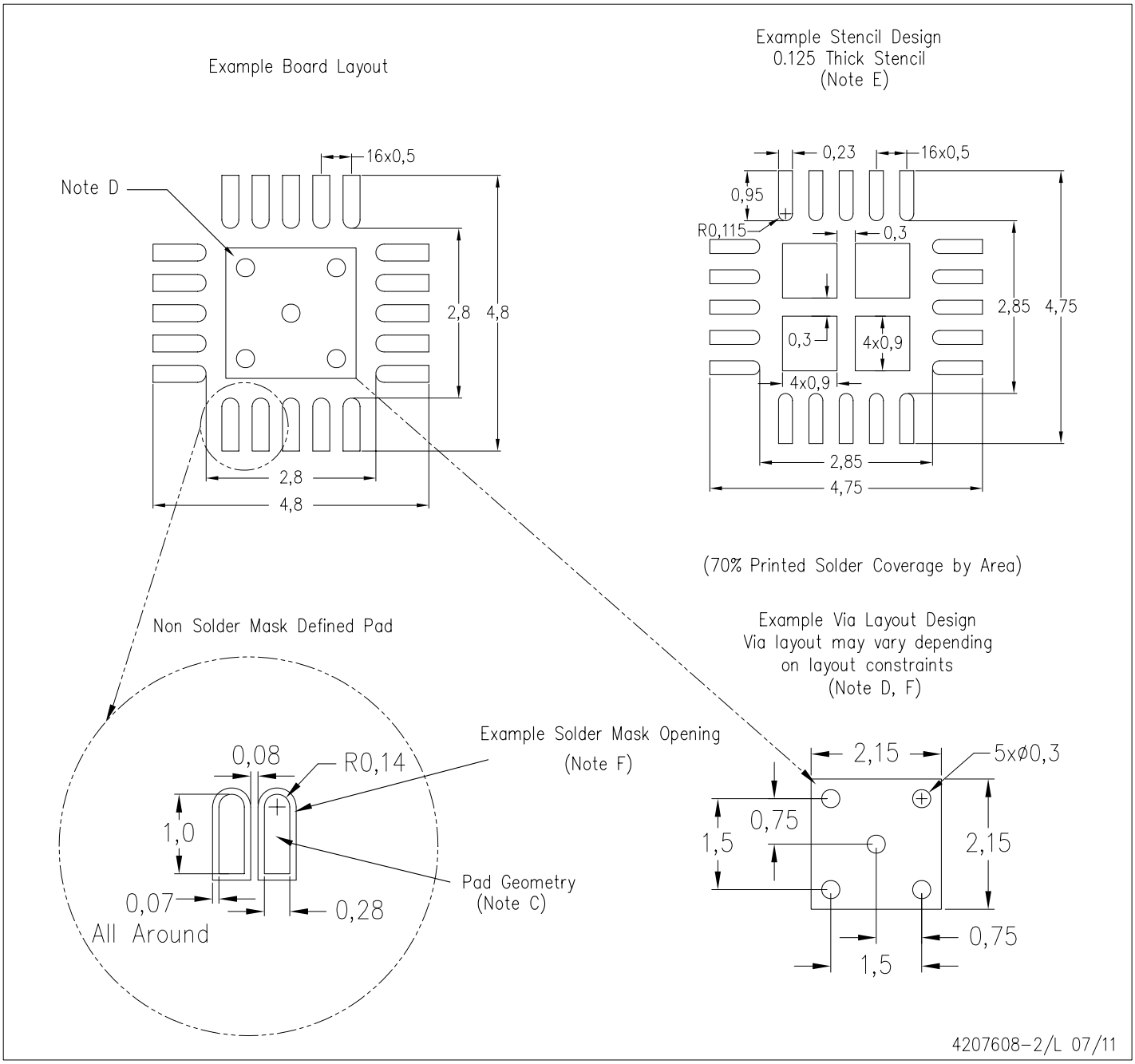
Exposed Thermal Pad Dimensions

4206346–2/W 07/11

NOTES: A. All linear dimensions are in millimeters

B. The Pin 1 Identification mark is an optional feature that may be present on some devices In addition, this Pin 1 feature if present is electrically connected to the center thermal pad and therefore should be considered when routing the board layout.

RGP (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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